



CJ40561 Series

■ INTRODUCTION:

The CJ40561 is a fully integrated high input voltage single-cell Li-Ion battery charger. The charger uses a CC/CV charge profile required by Li-Ion battery. The charger accepts an input voltage up to 26.5V but is disabled when the input voltage exceeds the OVP threshold, typically 10.5V, to prevent excessive power dissipation. The 26.5V rating eliminates the over-voltage protection circuit required in a low input voltage Charger.

The charge current and the full-of-charge (FOC) current are programmable with external resistors. When the battery voltage is lower than typically 2.55V(CJ40561-4.2), or 2.65V(CJ40561-4.35), the charger preconditions the battery with typically 47.5% of the programmed charge current. When the charge current reduces to the programmable FOC current level during the CV charge phase, an FOC indication is provided by the $\overline{\text{CHG}}$ pin, which is an open-drain output. An internal thermal foldback function protects the charger from any thermal failure.

Two indicator pins (PPR and CHG) allow simple interface to a microprocessor or LEDs. When no adapter is attached or when disabled, the charger draws less than 1 μ A leakage current from the battery.

■ APPLICATIONS:

- IOT Gadgets
- Wearable Devices
- Credential Keys
- Wireless Remote

■ FEATURES:

- 4.2V/4.35V Charge Voltage
- 5mA to 300mA Charger for Tiny Cell Li-Ion or Polymer Batteries
- Integrated Pass Element and Current Sensor
- No External Blocking Diode Required
- Low Component Count
- Programmable Charge Current
- Programmable Full-of-Charge Current
- Charge Current Thermal Foldback Protection
- 2.55V/2.65V Trickle Charge Threshold
- 10.5V Input Over-Voltage Protection
- 26.5V Maximum Voltage Power Input
- Power Presence and Charging Indications
- Less than 1 μ A Leakage Current off the Battery When No Input Power Attached or Charger Disabled
- Available in Green TDFN-2 \times 2-8L Package

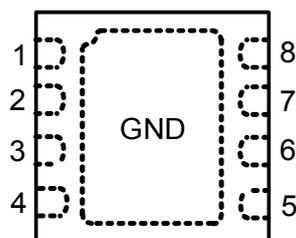
Electrical Characteristics

■ ORDERING INFORMATION

Device No.	Battery Float Voltage	Package	Packaging
CJ40561A420FB8	4.20V	TDFN2.0x2.0-8L	3000 parts per reel
CJ40561A435FB8	4.35V	TDFN2.0x2.0-8L	3000 parts per reel

(1)Contact Chippower to check availability of other battery float voltage versions or charge termination current versions.

■ PIN CONFIGURATION



DFN2X2-8L(Top View)

Table 1. Pin Description

PIN NO.	PIN NAME	FUNCTION
1	VIN	Power Input. The absolute maximum input voltage is 26.5V. A 1 μ F or larger value X5R ceramic capacitor is recommended to be placed very close to the input pin for decoupling purpose. Additional capacitance may be required to provide a stable input voltage. Adding a 1 Ω resistor in series with an X5R ceramic capacitor will minimize start-up voltage transients.
2	$\overline{\text{PPR}}$	Open-Drain Power Presence Indication. The open-drain MOSFET turns on when the input voltage is above the POR threshold but below the OVP threshold and off otherwise. This pin is capable to sink 15mA current to drive an LED. The maximum voltage rating for this pin is 5.5V. This pin is independent on the $\overline{\text{EN}}$ pin input.
3	$\overline{\text{CHG}}$	Open-Drain Charge Indication. This pin outputs a logic low when a charge cycle starts and turns to high impedance when the full-of-charge (FOC) condition is qualified. This pin is capable to sink 15mA current to drive an LED. When the charger is disabled, the $\overline{\text{CHG}}$ pin outputs high impedance.
4	$\overline{\text{EN}}$	Enable Input. This is a logic input pin to disable or enable the charger. Drive to high to disable the charger. When this pin is driven to low or left floating, the charger is enabled. This pin has an internal 200k Ω pull-down resistor.
5	GND	System Ground.
6	IMIN	Full-of-Charge (FOC) Current Programming Pin. Connect a resistor between this pin and the GND pinto set the FOC current. The FOC current IMIN can be programmed by the following equation

Electrical Characteristics

		$I_{MIN} = \frac{10960}{R_{IMIN}} \text{ (mA)}$ <p>where R_{IMIN} is in $k\Omega$.</p>
7	IREF	<p>Charge-Current Programming and Monitoring Pin. Connect a resistor between this pin and the GND pin to set the charge current limit determined by the following equation:</p> $I_{REF} = \frac{11980}{R_{IREF}} + 0.6 \text{ (mA)}$ <p>where R_{IREF} is in $k\Omega$. The resistor should be located very close to this pin. The IREF pin voltage also monitors the actual charge current during the entire charge cycle, including the trickle, constant-current, and constant-voltage phases. When disabled, $V_{IREF} = 0V$.</p>
8	BAT	<p>Charger Output Pin. Connect this pin to the battery. A $1\mu F$ or larger X5R ceramic capacitor is recommended for decoupling and stability purposes. When the \overline{EN} pin is pulled to logic high, the BAT output is disabled.</p>

■ ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified, $T_a=25^\circ C$)

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		V_{IN}	-0.3~28	V
PPR, CHG, EN, IMIN, IREF, BAT to GND		-	-0.3~6	V
Storage Temperature Range		T_{stg}	-40~+125	$^\circ C$
Package Power dissipation	TDFN2X2-8L	P_D	1000	mW
Operating Ambient Temperature		T_A	-40~85	$^\circ C$
Junction Temperature		T_j	-40~150	$^\circ C$
Storage Temperature		T_{stg}	-40~+125	$^\circ C$
Lead Temperature & Time		T_{solder}	260, 10s	$^\circ C$
ESD Susceptibility	HBM	-	4000	V
	MM	-	200	V

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNITS
Supply Voltage Range	V_{IN}	4.50~ 9.35	V
Maximum Supply Voltage	-	26.5	V
Programmed Charge Current	I_{BAT}	5~300	mA
Operating Temperature Range	T_{opr}	-40~+85	°C

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. CHIPPOWER recommends that all integrated circuits be handled with appropriate precautions.

Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

CHIPPOWER reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time

Electrical Characteristics

■ ELECTRICAL CHARACTERISTICS

($V_{IN}=5.0V$, $R_{IMIN} = 3M\Omega$, $T_a=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
POWER-ON RESET							
Rising POR Threshold	V_{POR}	$V_{BAT} = 3.0V$, $R_{IREF} = 602k\Omega$, use \overline{PPR} to indicate the comparator output.	3.21	3.95	4.55	V	
Falling POR Threshold			2.86	3.60	4.35	V	
VIN-BAT OFFSET VOLTAGE							
Rising Edge	V_{OS}	V_{BAT} forced to 4.5V, $R_{IREF} = 602k\Omega$, use \overline{PPR} pin to indicate the comparator output. ⁽¹⁾		110	200	mV	
Falling Edge			5	60		mV	
OVER-VOLTAGE PROTECTION							
Over-Voltage Protection Threshold	V_{OVP}	V_{BAT} forced to 4.4V, $R_{IREF} = 602k\Omega$, use \overline{PPR} to indicate the comparator output.	9.35	10.50	11.15	V	
	V_{OVPHYS}		245	340	430	mV	
STANDBY CURRENT							
BAT Pin Sink Current	$I_{STANDBY}$	The input is floating		0.1	0.6	μA	
		Charger disabled		0.2	1	μA	
VIN Pin Supply Current	I_{VIN}	V_{BAT} forced to 4.4V, $R_{IREF} = 301k\Omega$	charger disabled		160	250	μA
			charger enabled		220	320	μA
VOLTAGE REGULATION							
Output Voltage	CJ40561-4.20	V_{float}	$R_{IREF} = 301k\Omega$, $V_{IN} = 5V$, charge current = 3mA	4.152	4.20	4.248	V
	CJ40561-4.35			4.302	4.35	4.398	V
CHARGE CURRENT ⁽²⁾							
IREF Pin Output Voltage	V_{IREF}	$V_{BAT} = 3.8V$, $R_{IREF} = 602k\Omega$	1.162	1.21	1.262	V	
Constant Charge Current	I_{REF}	$R_{IREF} = 301k\Omega$, $V_{BAT} = 3.8V$	35	40	45	mA	
Trickle Charge Current	I_{TRIK}	$R_{IREF} = 301k\Omega$, $V_{BAT} = 2.4V$	12.5	18.75	25	mA	
Full-of-Charge Current	I_{MIN}	$R_{IREF} = 301k\Omega$	1	4	7	mA	
FOC Rising Threshold		$R_{IREF} = 301k\Omega$	22	31	40	mA	
PRECONDITIONING CHARGE THRESHOLD							

Electrical Characteristics

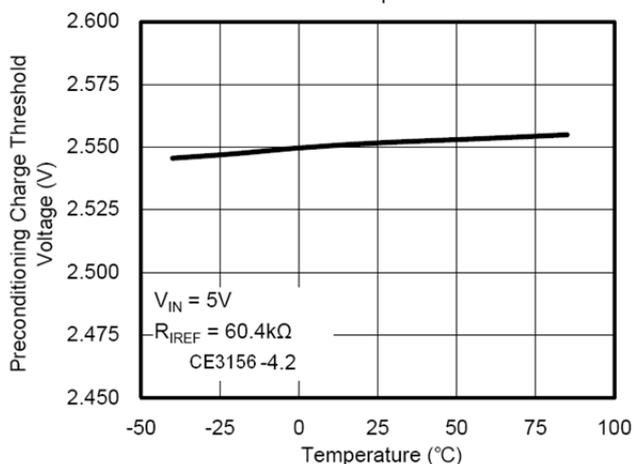
Preconditioning Charge Threshold Voltage	CJ40561-4.20	V_{MIN}	$R_{IREF} = 602k\Omega$		2.55		V
	CJ40561-4.35				2.65		V
Preconditioning Voltage Hysteresis		V_{MINHYS}	$R_{IREF} = 602k\Omega$		100		mV
INTERNAL TEMPERATURE MONITORING							
Charge Current Foldback Threshold		T_{FOLD}	V_{IN} from High to Low		115		°C
LOGIC INPUT AND OUTPUTS							
\overline{EN} Pin Logic Input High				1.6			V
\overline{EN} Pin Logic Input Low						0.8	V
\overline{EN} Pin Internal Pull-Down Resistance				150	200	250	k Ω
\overline{CHG} Pin On-Resistance when LOW			Pin voltage = 1V		42	67	Ω
\overline{CHG} Leakage Current when High Impedance			$V_{\overline{CHG}} = 5.5V$			20	μA
\overline{PPR} Pin On-Resistance when LOW			Pin voltage = 1V		42	67	Ω
\overline{PPR} Leakage Current when High Impedance			$V_{\overline{PPR}} = 5.5V$			20	μA

NOTES:

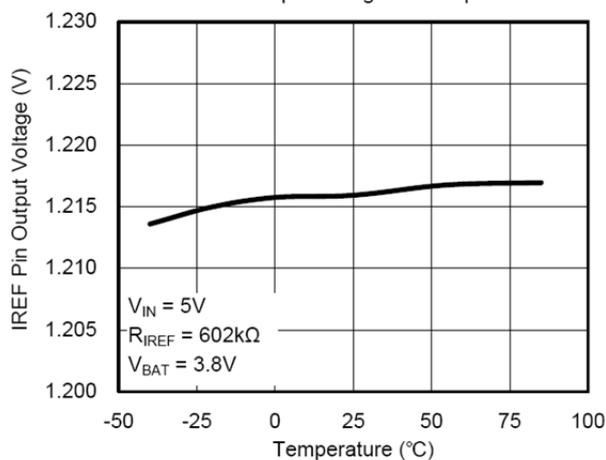
1. The 4.5V V_{BAT} is selected so that the \overline{PPR} output can be used as the indication for the offset comparator output indication. If the V_{BAT} is lower than the POR threshold, no output pin can be used for indication.
2. The charge current may be affected by the thermal foldback function.

Electrical Characteristics

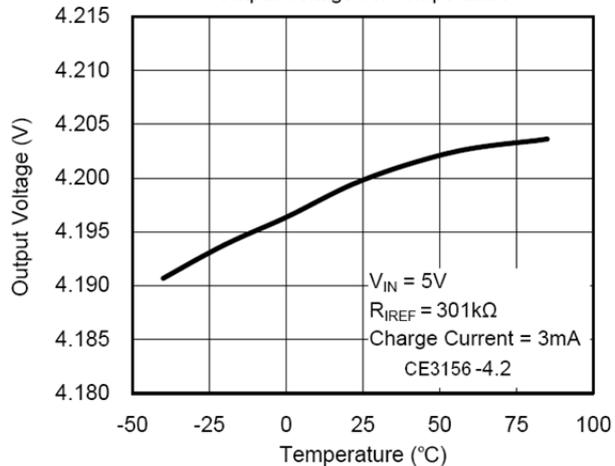
Preconditioning Charge Threshold Voltage vs. Temperature



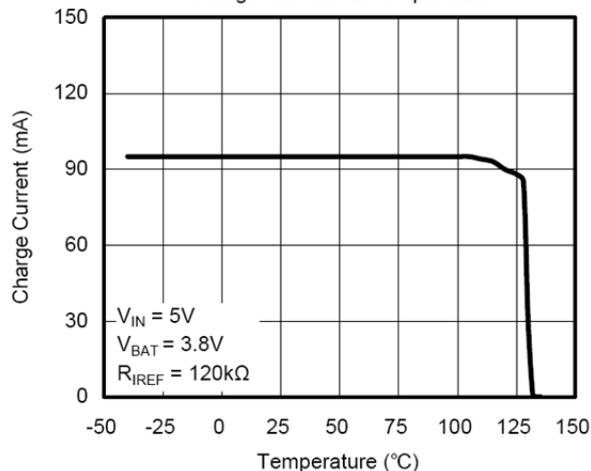
IREF Pin Output Voltage vs. Temperature



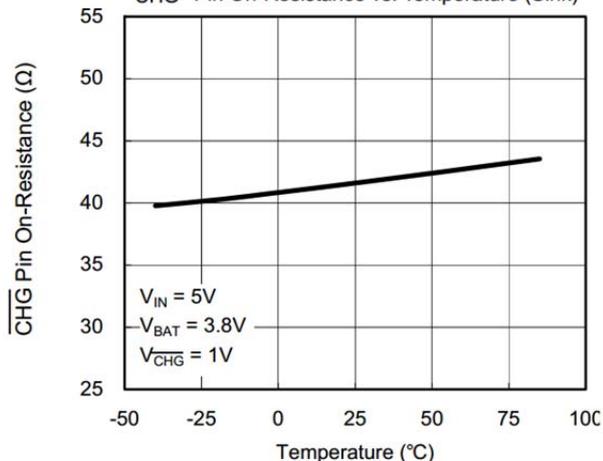
Output Voltage vs. Temperature



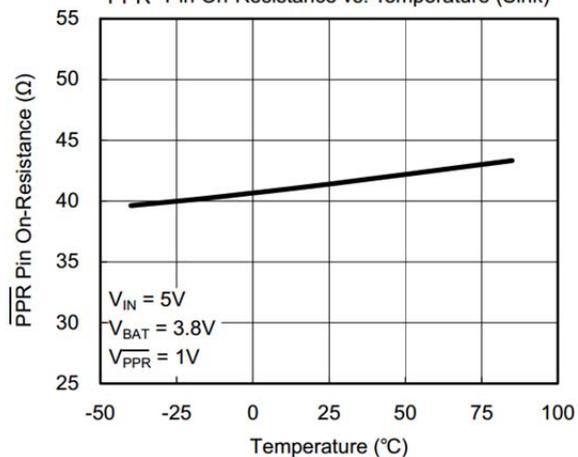
Charge Current vs. Temperature



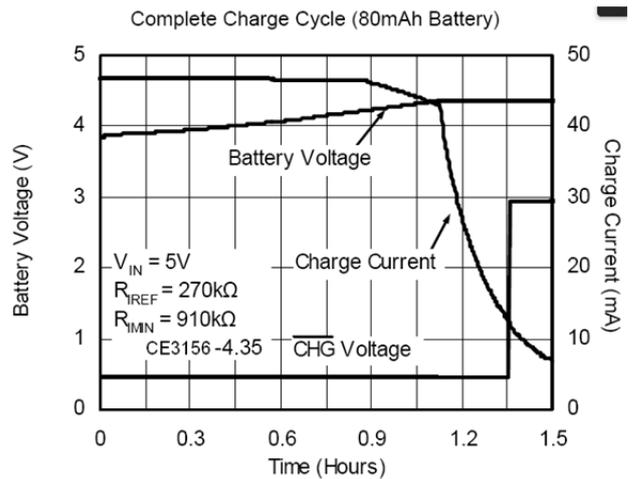
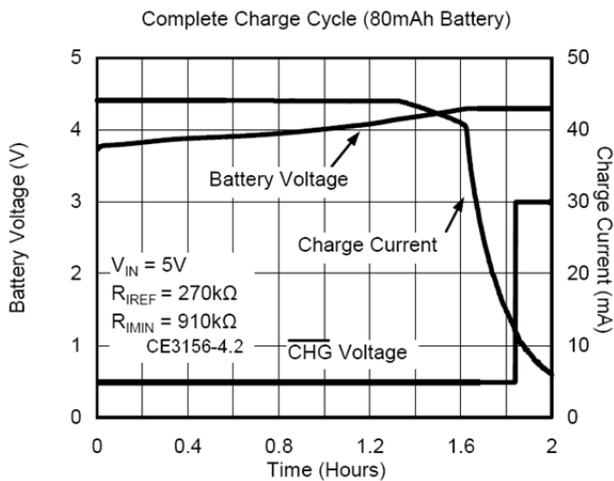
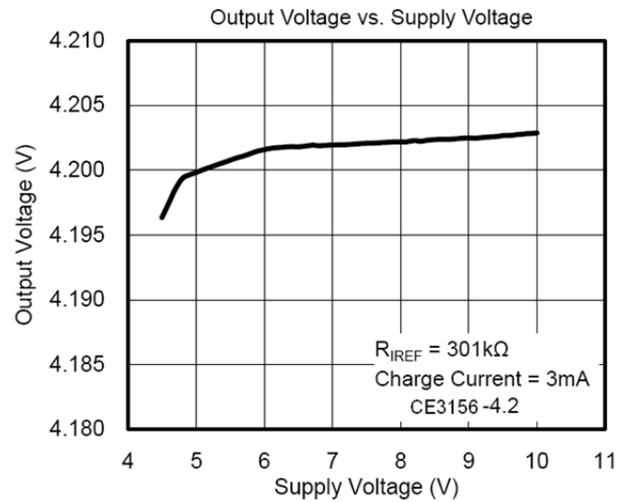
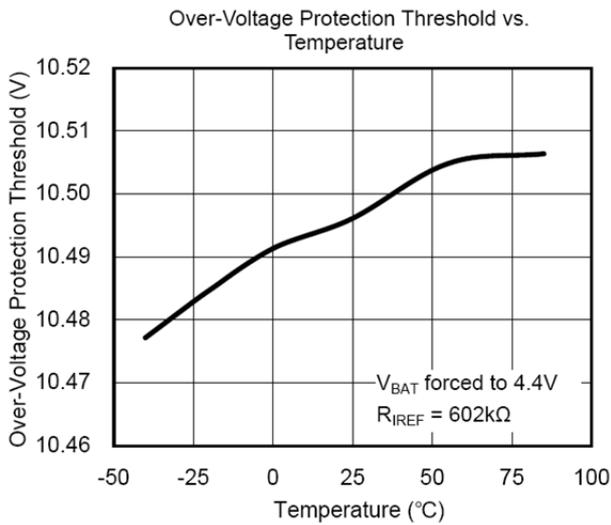
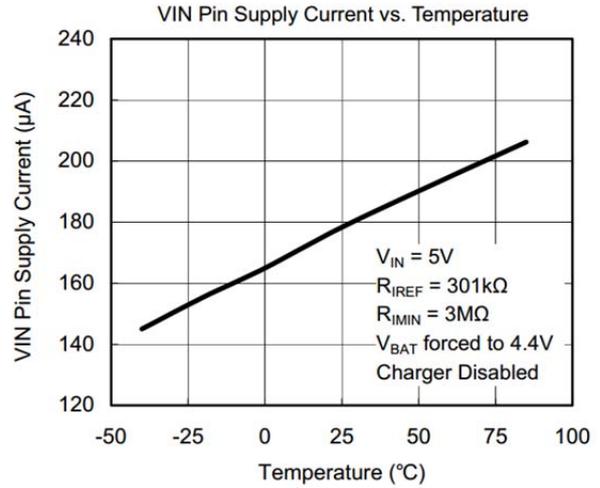
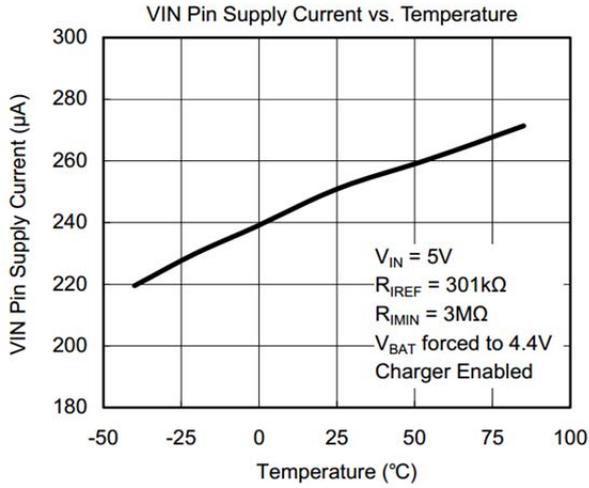
CHG Pin On-Resistance vs. Temperature (Sink)

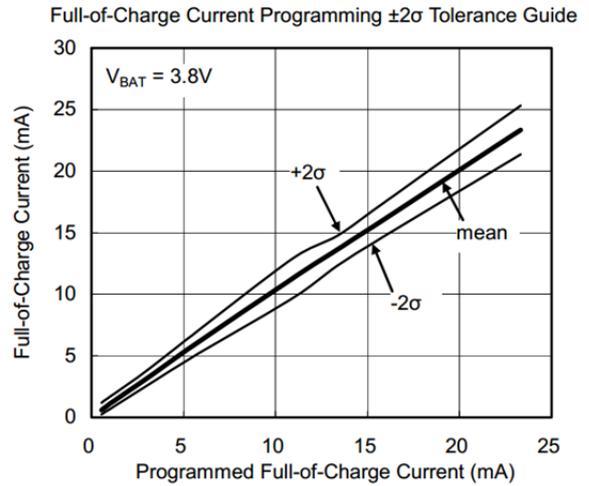
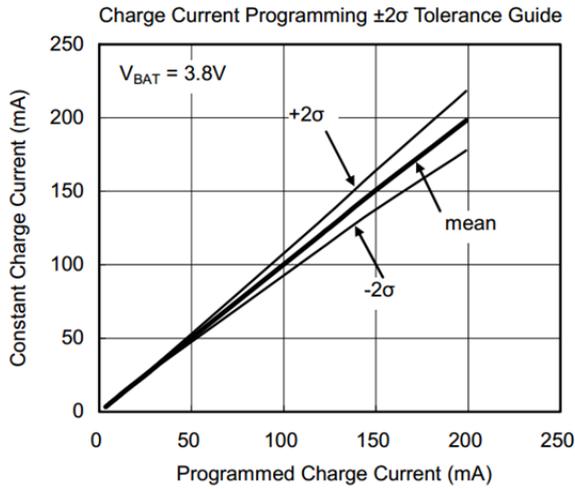


PPR Pin On-Resistance vs. Temperature (Sink)



Electrical Characteristics





■ TYPICAL APPLICATION CIRCUIT

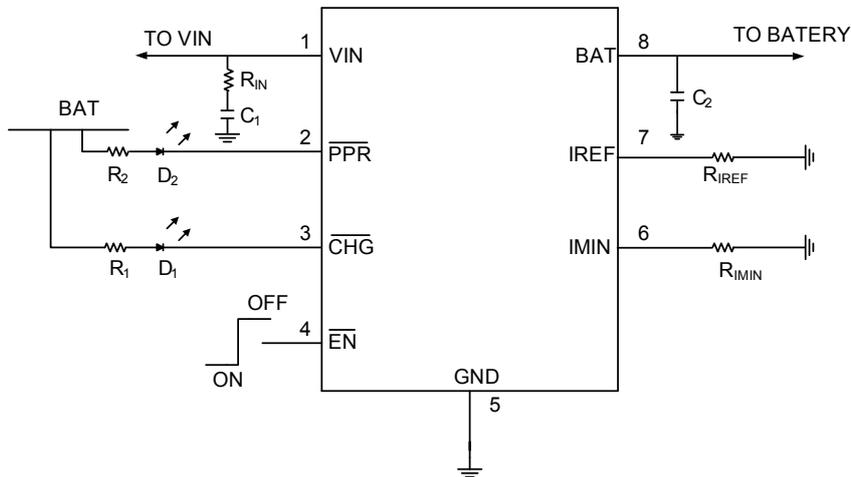


Figure1 Typical Application Circuit Interfacing to Indication LEDs

COMPONENT DESCRIPTION FOR Figure1

PART	DESCRIPTION
C1	1 μ F X5R ceramic cap
C2	1 μ F X5R ceramic cap
R _{IREF}	301k Ω , for 40mA charge current
R _{IMIN}	3M Ω , for 4mA FOC current
D1,D2	LEDs for indication
R1,R2	100k Ω , 5% resistor
R _{IN}	1 Ω resistor

Adding a 1 Ω resistor in series with an X5R ceramic capacitor will minimize start-up voltage transients.

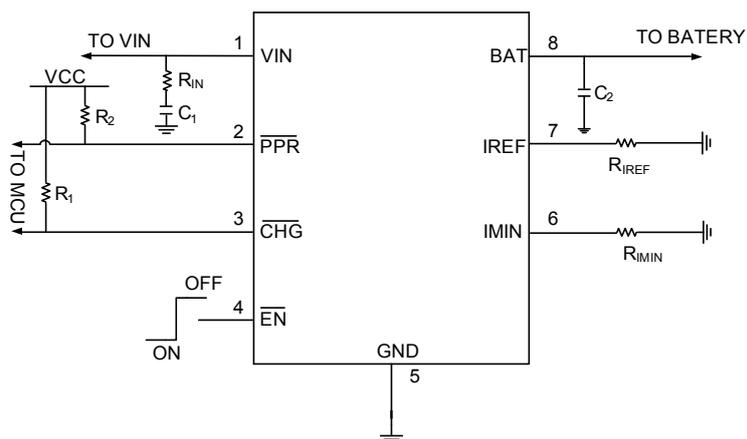


Figure2 Typical Application Circuit with the Indication Signals Interfacing to an MCU

COMPONENT DESCRIPTION FOR Figure2

PART	DESCRIPTION
C1	1μF X5R ceramic cap
C2	1μF X5R ceramic cap
R _{IREF}	301kΩ, for 40mA charge current
R _{IMIN}	3MΩ, for 4mA FOC current
R1,R2	100kΩ , 5% resistor
R _{IN}	1Ω resistor

Adding a 1Ω resistor in series with an X5R ceramic capacitor will minimize start-up voltage transients.

■ TYPICAL CHARGE PROFILE

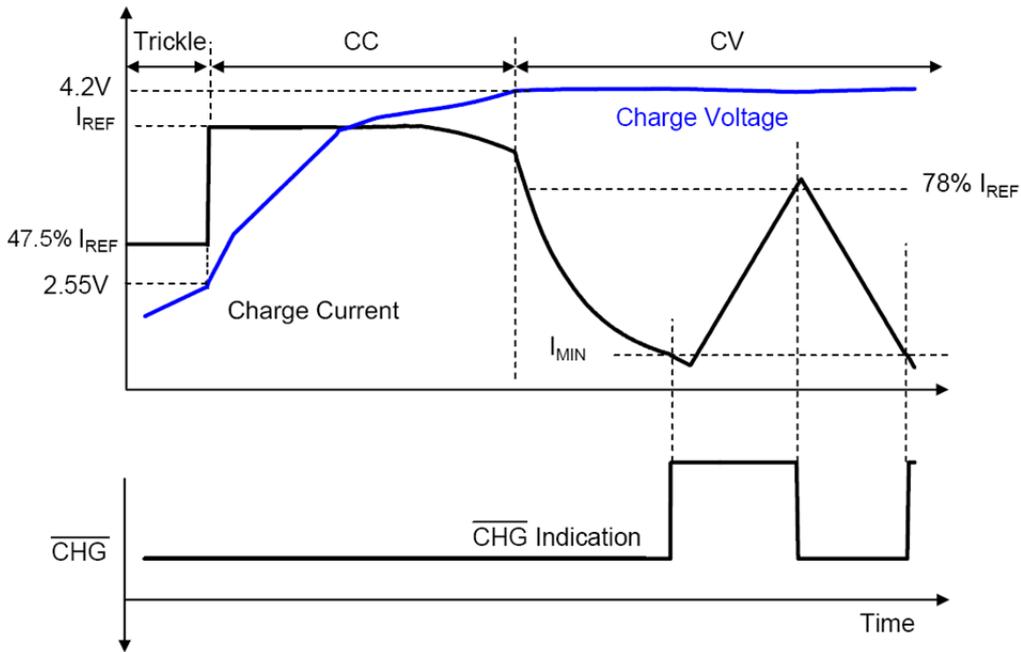


Figure3 Typical Charge Profile

■ FUNCTIONAL BLOCK DIAGRAM

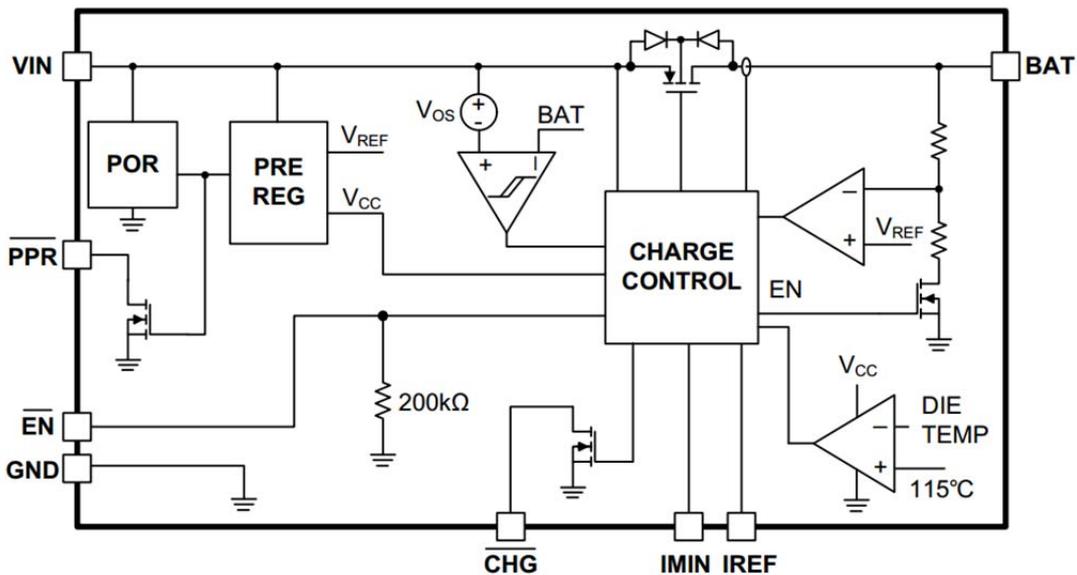


Figure4 Functional Block Diagram

■ OPERATION INFORMATION

The CJ40561 charges a Li-Ion battery using a CC/CV profile. The constant current IREF is set with the external resistor R_{IREF} (see Figure 1) and the constant voltage is fixed at 4.2V or 4.35V. If the battery voltage is below a typical 2.55V, or

2.65V trickle charge threshold, the CJ40561 charges the battery with a trickle current of 47.5% of IREF until the battery voltage rises above the trickle charge threshold. Fast charge CC mode is maintained at the rate determined by programming IREF until the cell voltage rises to

4.2V or 4.35V. When the battery voltage reaches 4.2V or 4.35V, the charger enters a CV mode and regulates the battery voltage at 4.2V or 4.35V to fully charge the battery without the risk of over charge. Upon reaching an full-of-charge (FOC) current, the charger indicates the charge completion with the $\overline{\text{CHG}}$ pin, but the charger continues to output the 4.2V or 4.35V voltage. Figure 3 shows the typical charge waveforms after the power is on.

The FOC current level I_{MIN} is programmable with the external resistor R_{IMIN} (see Figure 1). The $\overline{\text{CHG}}$ pin turns to low when the trickle charge starts and rises to high impedance at the FOC. After the FOC is reached, the charge current has to rise to typically 78% of I_{REF} for the $\overline{\text{CHG}}$ pin to turn on again, as shown in Figure 3. The current surge after FOC can be caused by a load connected to the battery.

A thermal foldback function reduces the charge current any time when the die temperature reaches typically 115°C. This function guarantees safe operation when the printed circuit board (PCB) is not capable of dissipating the heat generated by the linear charger. The CJ40561 accepts an input voltage up to 26.5V but disables charging when the input voltage exceeds the OVP threshold, typically 10.5V, to protect against unqualified or faulty AC adapters.

PPR Indication

The $\overline{\text{PPR}}$ pin is an open-drain output to indicate the presence of the AC adapter. Whenever the input voltage is higher than the POR threshold, the $\overline{\text{PPR}}$ pin turns on the internal open-drain MOSFET to indicate a logic low signal, independent on the $\overline{\text{EN}}$ pin input. When the internal open-drain FET is turned off, the $\overline{\text{PPR}}$ pin leaks less than 20µA current. When turned on, the $\overline{\text{PPR}}$ pin is able to sink at least 15mA current under all operating conditions. The $\overline{\text{PPR}}$ pin can be used to drive an LED (see Figure 1) or to interface with a micro-processor.

Power Good Range

The power good range is defined by the following three conditions:

1. $V_{\text{IN}} > V_{\text{POR}}$
2. $V_{\text{IN}} - V_{\text{BAT}} > V_{\text{OS}}$
3. $V_{\text{IN}} < V_{\text{OVP}}$

where the V_{OS} is the offset voltage for the input and output voltage comparator, discussed shortly, and the V_{OVP} is the over-voltage protection threshold given in the Electrical Characteristics table. All V_{POR} , V_{OS} , and V_{OVP} have hysteresis, as given in the Electrical Characteristics table. The charger will not charge the battery if the input voltage is not in the power good range.

Input and Output Comparator

The charger will not be enabled unless the input voltage is higher than the battery voltage by an offset voltage V_{OS} . The purpose of this comparator is to ensure that the charger is turned off when the input power is removed from the charger. Without this comparator, it is possible that the charger will fail to power down when the input is removed and the current can leak through the PFET pass element to continue biasing the POR and the Pre-Regulator blocks.

Dropout Voltage

The constant current may not be maintained due to the $R_{\text{DS(ON)}}$ limit at a low input voltage. The worst case $R_{\text{DS(ON)}}$ is at the maximum allowable operating temperature.

$\overline{\text{CHG}}$ Indication

The $\overline{\text{CHG}}$ is an open-drain output capable of sinking at least 15mA current when the charger starts to charge, and turns off when the FOC current is reached. The $\overline{\text{CHG}}$ signal is interfaced either with a microprocessor GPIO or an LED for indication.

$\overline{\text{EN}}$ Input

$\overline{\text{EN}}$ is an active-low logic input to enable the charger. Drive the $\overline{\text{EN}}$ pin to low or leave it floating to enable the charger. This pin has a 200kΩ internal pull-down resistor so when left it floating, the input is equivalent to logic low. Drive this pin to high to disable the charger. The threshold for high is given in the Electrical Characteristics table.

IREF Pin

The IREF pin has the two functions as described

in the Pin Description section. When monitoring the charge current, the accuracy of the IREF pin voltage vs. the actual charge current has the same accuracy as the gain from the IREF pin current to the actual charge current.

Operation without the Battery

The CJ40561 relies on a battery for stability and works under LDO mode if the battery is not connected. With a battery, the charger will be stable with an output ceramic decoupling capacitor in the range of 1 μ F to 200 μ F. In LDO mode, its stability depends on load current, C_{OUT}, etc. The maximum load current is limited by the dropout voltage, the programmed IREF and the thermal foldback.

Thermal Foldback

The thermal foldback function starts to reduce the charge current when the internal temperature reaches a typical value of 115°C.

■ APPLICATION INFORMATION

Design of IREF, IMIN and $\overline{\text{CHG}}$ Indication

A higher IREF charges quicker, at the penalty of reduced battery life, so the maximum IREF should be designed to follow battery vendor's instruction for a given battery life expectation.

IMIN is the end of charge current when $\overline{\text{CHG}}$ indicates a full of charge condition. All current out of the CJ40561 BAT pin should be counted into IMIN, including load current and the indication LED currents. As illustrated in Figure 3, the CJ40561 continues to supply current unless it is disabled by EN pulled high, regardless of the status of $\overline{\text{CHG}}$ pin. When charge current ever goes lower than IMIN, $\overline{\text{CHG}}$ pin stays high impedance until the charge current goes higher than 78% of IREF, which is another factor to consider in design of IREF, IREF should be high enough to so that 78% of IREF is higher than the current that is designed not to initiate $\overline{\text{CHG}}$ indication, while is low enough to assure the power source could deliver higher than 78% of IREF to initiate $\overline{\text{CHG}}$ indication.

Input Capacitor Selection

The input capacitor is required to suppress the power supply transient response during transitions. Mainly this capacitor is selected to avoid oscillation during the startup when the input supply is passing the POR threshold and the VIN-BAT comparator offset voltage. When the battery voltage is above the POR threshold, the VIN -VBAT offset voltage dominates the hysteresis value.

Typically, a 1 μ F X5R ceramic capacitor should be sufficient to suppress the power supply noise. However, caution must be exercised when using multilayer ceramic capacitors (MLCC). Because of the self-resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as connecting the input to a live power source. Adding a 1 Ω resistor in series with an X5R ceramic capacitor will minimize start-up voltage transients.

Output Capacitor Selection

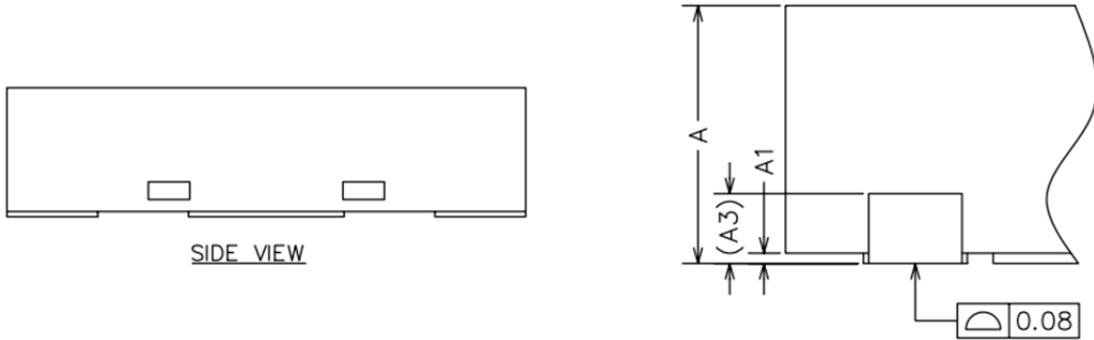
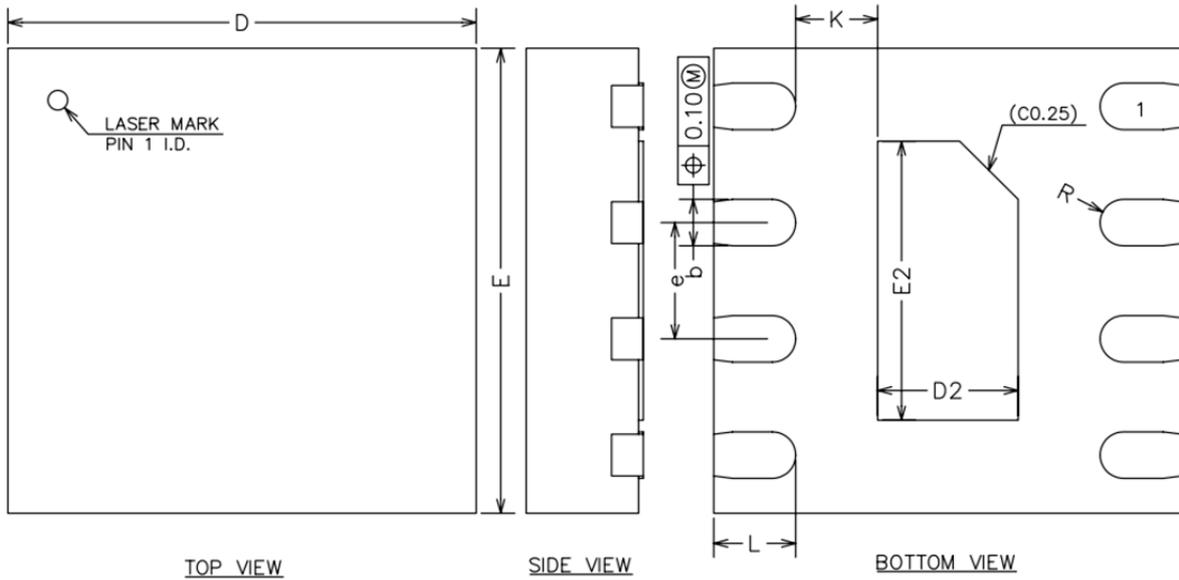
The criterion for selecting the output capacitor is to maintain the stability of the charger as well as to bypass any transient load current. The minimum capacitance is a 1 μ F X5R ceramic capacitor. The actual capacitance connected to the output is dependent on the actual application requirement.

Layout Guidance

The CJ40561 uses thermally-enhanced TDFN package that has an exposed thermal pad at the bottom side of the package. The layout should connect as much as possible to copper on the exposed pad.

Typically the component layer is more effective in dissipating heat. The thermal impedance can be further reduced by using other layers of copper connecting to the exposed pad through a thermal via array. Each thermal via is recommended to have 0.3mm diameter and 1mm distance from other thermal via.

TDFN2X2-8L Package Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20REF		
b	0.15	0.20	0.25
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.50	0.60	0.70
E2	1.10	1.20	1.30
e	0.40	0.50	0.60
K	0.20	-	-
L	0.30	0.35	0.40
R	0.09	-	-

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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